

CLAIMS:

What is claimed is:

1 1. A method for full speculation of instruction
2 processing in a multiprocessor data processing system
3 comprising:

4 issuing from a processor a barrier operation on a
5 system bus of said data processing system; and

6 executing operations associated with instructions
7 sequentially following said barrier operation in an
8 instruction sequence prior to completion of said barrier
9 operation.

1 2. The method of Claim 1, wherein said executing step
2 executes said operations, prior to said issuing step.

1 3. The method of Claim 1, wherein said executing step
2 further comprises:

3 issuing a load request for data;

4 responsive to a return of said data, immediately
5 forwarding said data to a register of said processor; and

6 providing said data to subsequent processes that
7 utilize said data.

1 4. The method of claim 3, further comprising setting a
2 flag within said register when said barrier operation has
3 not yet completed, wherein said flag indicates that each
4 instruction executed and each result generated by said
5 subsequent processes and stored within said register is
6 speculative, pending a completion of said barrier
7 operation.

1 5. The method of Claim 4, further comprising:

2 monitoring for said completion of said barrier
3 operation;

4 responsive to said completion, resetting said flag
5 and concurrently indicating said register as non-
6 speculative.

1 6. The method of Claim 5, wherein further, when an
2 invalidate is received prior to said completion, said
3 processor discards said data and each of said result from
4 said register.

1 7. The method of Claim 6, wherein said operations
2 include load requests and branch instructions, and
3 wherein further said method provides embedded branch
4 speculation within said operations and speculative load
5 request issuing within a branch path.

1 8. A multiprocessor computer system comprising:

2 a plurality of processors interconnected by a system
3 bus, wherein said processors including a first processor
4 that speculatively issues load requests and processes
5 subsequent instructions utilizing data returned by said
6 load request before a completion of a barrier operation
7 that is sequentially before said load requests and
8 subsequent instructions in an instruction sequence; and

9 a memory hierarchy connected to said plurality of
10 processors via said system bus that sources said data.

1 9. The multiprocessor computer system of Claim 8,
2 wherein said first processor comprises a load/store unit
3 with logic that controls issuing of load and store
4 instructions before completion of a preceding barrier
5 operation to provide said data to a register of said
6 first processor prior to a return of an acknowledgment
7 for said preceding barrier operations.

1 10. The multiprocessor computer system of claim 8,
2 wherein said first processor further comprises:

3 execution units that processes instructions that
4 utilize said data when said data is placed in said
5 register; and

6 logic, affiliated with said register, that sets a
7 flag within said register when a value resulting from

8 executing said instructions is placed in said register
9 prior to said completion, wherein said flag messages to
10 the execution units that said instruction and said
11 results are speculative, pending a completion of said
12 barrier operation.

1 11. The multiprocessor computer system of claim 8,
2 wherein said logic further resets said flag responsive to
3 said completion.

1 12. The multiprocessor computer system of claim 11,
2 wherein said first processor further comprises a
3 plurality of execution queues and logic for setting a bit
4 associated with an entry of said queues to indicate
5 whether an instruction placed in said entry is
6 speculative with respect to said barrier operation.

1 13. The multiprocessor computer system of claim 11,
2 wherein said first processor further comprises a
3 plurality of execution queues and logic for setting a bit
4 associated with an entry of said queues to indicate
5 whether an instruction placed in said entry is
6 speculative with respect to an unresolved branch
7 instruction that precedes said instruction in said
8 instruction sequence.

1 14. A processor comprising:

2 a plurality of execution units including a
3 load/store unit, wherein said load/store unit,
4 speculatively executes load requests and offer other
5 execution into speculative execute other instructions
6 before completion of a barrier operation that precedes
7 said load requests and other instructions in an
8 instruction sequence;

9 a rename register that includes a plurality of
10 entries, wherein each entry has a speculation flag and an
11 associated general purpose register identifier; and

12 logic for setting said speculation flag to indicate
13 when a value stored in said entry is speculative, pending
14 completion of said barrier operation.

1 15. The processor of Claim 14, wherein said load/store
2 unit provides data returned by said load requests
3 immediately to an entry of said rename register for
4 utilization within subsequent processes that require said
5 data.

1 16. The processor of Claim 15, wherein said load/store
2 unit messages said execution units and said logic when
3 said barrier operation completes.

1 17. The processor of Claim 16, wherein, said logic,
2 responsive to a receipt of a message indicating
3 successful completion of said barrier operation, resets
4 each flag associated with a register entry that was
5 speculative with respect to said barrier operation.

1 18. The processor of Claim 17, further comprising:

2 a plurality of issue queues associated with said
3 execution units in which instructions to be executed are
4 placed; and

5 logic for indicating that a particular instruction
6 within one of said issue queues is speculative with
7 respect to the barrier operation.

1 19. The processor of Claim 17, further comprising:

2 a plurality of issue queues associated with said
3 execution units in which instructions to be executed are
4 placed; and

5 logic for indicating that a particular instruction
6 within one of said issue queues is speculative with
7 respect to an unresolved branch instruction that precedes
8 said instruction within said instruction sequence.

1 20. The processor of Claim 18, further comprising:

2 an enhanced internal instruction set architecture
3 that includes a setable bit, which indicates whether an
4 instruction is speculative, wherein said logic sets said
5 setable bit responsive to whether said barrier operation
6 has completed; and

7 when said barrier operation has completed, said
8 logic resets said bit.

1 21. The processor of Claim 18, wherein said issue queues
2 includes a speculation bit associated with each entry
3 location, wherein said speculation bit is set by said
4 logic when said particular instruction is placed in an
5 associated entry location, and reset only when said
6 barrier operation has successfully completed.

1 22. A data processing system comprising:

2 a memory;

3 at least two processors interconnected to each other
4 and said memory via a system bus, wherein a first
5 processor comprises:

6 a plurality of execution units including a
7 load/store unit, wherein said load/store unit
8 speculatively executes load requests and offer other
9 execution into speculative execute other
10 instructions before completion of a barrier
11 operation that precedes said load requests and other
12 instructions in an instruction sequence;

13 a rename register that includes a plurality of
14 entries, wherein each entry has a speculation flag
15 and an associated general purpose register
16 identifier; and

17 logic for setting said speculation flag to
18 indicate when a value stored in said entry is
19 speculative, pending completion of said barrier
20 operation.

1 23. The data processing system of Claim 22, wherein said
2 load/store unit provides data returned by said load
3 requests immediately to an execution unit of said
4 processor for utilization within subsequent processes
5 that require said data.

1 24. The data processing system of Claim 23, wherein said
2 load/store unit messages said execution units and said
3 logic when said barrier operation completes.

1 25. The data processing system of Claim 24, wherein,
2 said logic, responsive to a receipt of a message
3 indicating successful completion of said barrier
4 operation, resets each flag associated with a register
5 entry that was speculative with respect to said barrier
6 operation.

1 26. The data processing system of Claim 25, further
2 comprising:

3 a plurality of issue queues associated with said
4 execution units in which instructions to be executed are
5 placed; and

6 logic for indicating that a particular instruction
7 within one of said issue queues is speculative with
8 respect to the barrier operation.

1 27. The data processing system of Claim 26, further
2 comprising:

3 an enhanced internal instruction set architecture
4 that includes a settable bit, which indicates whether an

5 instruction is speculative, wherein said logic sets said
6 setable bit responsive to whether said barrier operation
7 has completed; and

8 when said barrier operation has completed, said
9 logic resets said bit.

1 28. The data processing system of Claim 26, wherein said
2 issue queues includes a speculation bit associated with
3 each entry location, wherein said speculation bit is set
4 by said logic when said particular instruction is placed
5 in an associated entry location, and reset only when said
6 barrier operation has successfully completed.